Name:

Student Number:

Instructions

Write or draw your answer immediately below the corresponding question inside the given space such as the box surrounding these instructions.

The space provided is more than sufficient: do not write extended answers or on the margins or the backside of the paper. Text or figures outside the given space will be disregarded in evaluation.

Leave these pages and these pages only to the exam supervisor when you have finished or the examination time is over.

Maximum points for each of the six questions are given in brackets at the end of the question. The second and third questions include clearly separated parts marked with gray for which you can get extra points.

You have three hours to complete leaving you an average of thirty minutes per question: use your time wisely.

(6 points)

1. Explain the following through comparison.

a) Instruction set architecture (ISA) ***versus*** microarchitecture

b) Sign extension ***versus*** zero padding on the leftmost bits

c) Latency ***versus*** throughput in the context of processors

d) Interrupt ***versus*** trap

e) Cache miss ***versus*** page fault

f) Bus ***versus*** Network-on-chip (NoC)

(4 points)

2. Fill in the table of addressing modes commonly supported by RISC processors below.

In the first column from the left, the name of the addressing mode is given
In the second column from the left, write down how address is formed in each mode.
In the third column from the left, list instructions that typically use the addressing mode.
In the fourth column from the left, indicate what type(s) of content the mode is useful for.

Pseudo-direct addressing is slightly less common, while indexed addressing and update addressing are supported, e.g., by IBM's Power architectures. Fill in the three additional rows with the same information about these addressing modes. (+ 3 extra points)

Addressing Mode	Address Calculation (address = ?)	Typical Instructions (list of mnemonics)	Addressed Content (instructions, data)
Immediate Addressing			
PC-relative Addressing			
Register Addressing			
Base Addressing			
Pseudo-direct Addressing			
Indexed Addressing			
Update Addressing			

(4 points)

3. Fill in the table of pipeline hazards below.

In the first column from the left, name the three main categories of pipeline hazards.
In the second column from the left, formally describe what causes each type of hazard.
In the third column from the left, identify types of instructions that can cause these hazards.
In the fourth column from the left, list resolving techniques for each type of hazard.

With out-of-order execution there are three relevant subcategories of one main category of pipeline hazards. Name the three subcategories in the leftmost column and list their resolving techniques in the rightmost column of the three additional rows. (+ 3 extra points)

Hazard Type	Cause	Instruction Types	Resolving Techniques

(5 points)

4. Sketch a rough block diagram of a typical uniprocessor system identifying the two main parts of the processor. Depict the rest of the system with typical memory hierarchy.

(5 points)

5. Sketch a rough block diagram of a typical five-stage RISC pipeline. Associate the most important resources with each stage.

(6 points)

6.

a) What does Amdahl's law suggest?

b) How are pipeline bubbles formed?

c) How do fully associative, set associative, and direct mapped caches differ from each other?

d) What is the difference between write back and write through caches?

e) Explain how DMA operations proceed in steps from start to finish using correct terminology.