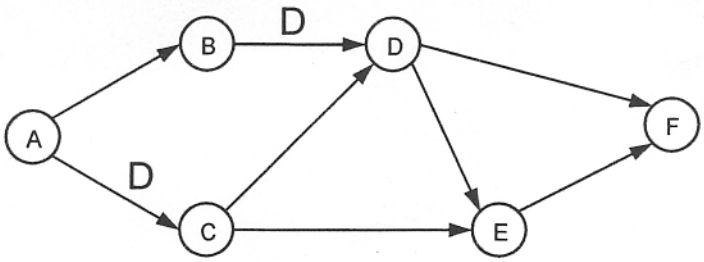
TKT-1560 DIGITAL DESIGN III

exam April 3 2006

1) Consider the DFG below. Assume the execution time of T for each node. a) What is the maximum achievable sample rate in this system? b) Place pipelining registers such that the sample rate of this system is about $1/T$ and latency is minimized.



2) Use forward backward register allocation technique to construct a hardware structure for the following data reordering over two inputs and outputs:

(0,1,2,3,4,5,6,7) -> (0,4,1,5,2,6,3,7)

i.e., samples in the left are fed into input and they are in the output in the order in the right. Two parallel inputs, thus 0 and 1 are fed to the system in the first cycle, 2 and 3 at the second cycle, etc.

3) Find the minimum unfolding factor J for the following DFG such that the J-unfolded DFG can be retimed so that the critical path of this unfolded and retimed DFG is JT_∞.