Table I: Table of instructions

General issues: 16 general purpose registers, 16-bit 2's complement data

INSTRUCTION	ADDRESSING MODES, LIMITATIONS, ETC.
Add	2 source and 1 destination registers
Add with carry	2 source and 1 destination registers
Subtract	2 source and 1 destination registers
Multiply	Mixture of signed and unsigned operands. 2 source and 1 **double** destination regs.
Logical shift	1 src, 1 dest reg, ±15 bit shifts from instruction
Logical shift on register	1 src, 1 dest reg, 1 shift-amount register
AND	2 source and 1 destination registers
OR	2 source and 1 destination registers
XOR	2 source and 1 destination registers
NOT	1 source and 1 destination registers
Conditional branch	Up to 7 conditions, PC-relative branch in ±255 range
Unconditional branch	PC-relative branch in ±255 range
Conditional branch on register	Up to 7 conditions, 1 reg. for branch address
Unconditional branch on register	1 reg. for branch address
Conditional branch and link on register	Up to 7 conditions, 1 reg. for branch address, 1 link register
Unconditional branch and link on register	1 reg. for branch address, 1 link register
Load	Register indirect with possible post-inc/dec, 1 dest reg.
Store	Register indirect with possible post-inc/dec, 1 src reg.
Load immediate	Signed ±127 immediate, 1 dest reg.
Register – register move	1 src and 1 dest reg.
No operation	

Table II: Instruction statistics

Static operation counts		
Operation	Times	Percentage
Add	2872	27.62
Load	1798	17.29
Logical	976	9.38
Subtract	941	9.05
Branch	777	7.47
Return	705	6.78
Store	632	6.08
Multiply	580	5.58
Compare	532	5.12
Call	379	3.64
Divide	208	2.00
TOTAL	10400	100.00