**TIE-50406 DSP Implementations**
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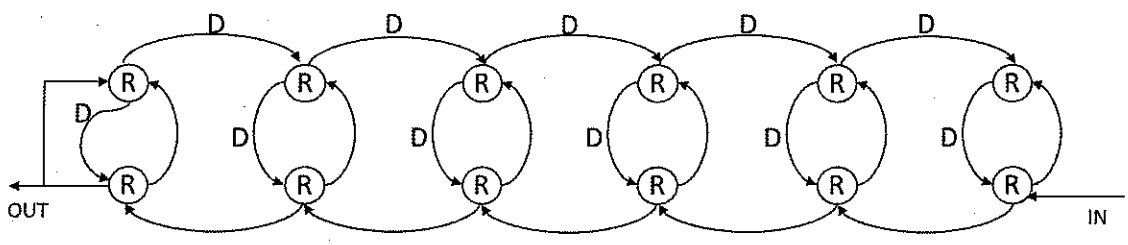
Exam Dec 20, 2017
**Calculators and dictionaries are allowed**

1. Explain shortly (1 point each):
   a) IEEE-754 denormal numbers
   b) Convergent rounding
   c) Saturation arithmetic
   d) An *enabled* node (in SDF graphs)
   e) Periodic schedule (in SDF)
   f) Inter-iteration precedence constraint

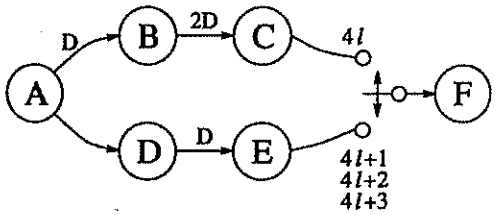
2. A DSP application is implemented on a 32-bit processor, which has only 32-bit registers, 32-bit memory system, and 32-bit arithmetic units. The piece of C code below shows a part of the implementation. Variables *x*, *w*, *s*, and *result* use the same fractional number representation.
   a) What is the number representation used? (1 point)
   b) Explain why s[k] is shifted (1 point)
   c) Explain why 16384 is added to y (1 point)
   d) Explain why y+16384 is shifted? (1 point)
   e) In the code, there is a possibility for overflow. Revise the code to avoid the overflow. Assume that coefficient *w* never gets value -1. (2 points)

```
int y, x[16], w[16], s[16], result;
.
.
.
y = 0;
for (int k=0; k<16; k++){
    y = y + w[k]*x[k] + (s[k] << 15);
}
result = (y + 16384) >> 15;
```

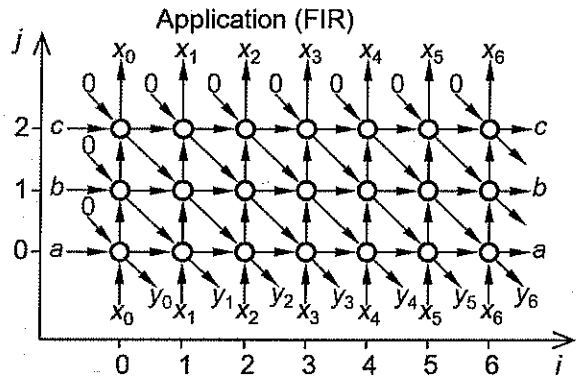
3. Consider the 6th order orthogonal filter structure shown below. All operations in this structure are CORDIC rotation operations. Assume that each CORDIC rotation operation requires 10 ns.
   a) Calculate the iteration bound of this filter (2 points)
   b) Show the critical path of this filter (1 point)
   c) Manually pipeline and/or retime the filter structure to achieve a critical path of computation 20 ns. Show all the cutset locations used for retiming explicitly. (3 points)



**4.** Perform unfolding by factor 2 for the DFG below (6 points)




**5.** Consider the FIR application dependency graph below




| Edge Mapping | | |
|---|---|---|
| **e** | **$p^Te$** | **$s^Te$** |
| | | |
| | | |
| | | |

a) For the FIR application, draw the systolic design α with $\mathbf{d} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$, $\mathbf{p}^T = [0\ 1]$, $\mathbf{s}^T = [2\ 1]$ (3 points)

b) What is the hardware utilization efficiency (HUE) of the design α? (1 point)

c) Construct the regular iterative algorithm (RIA) description of the FIR application (1 point)

d) Draw the reduced dependence graph (RDG) of the FIR application (1 point)