Name: _____

Student no.   _____

Final Exam: Answer every question

2nd Midterm Exam: Answer only questions 3-5

Made by: Arto Perttula

Students can use **any calculator** or dictionary.

Moreover, each student can have 1 A4 sheet of **own notes**. There are no restrictions about their style and they are not collected.

Students can do anything they wish with the exam paper.

In addition to text, use figures, tables, equations, and examples in your answers.

In logic diagrams, you can use basic gates (AND, OR...), flip-flops, multiplexers, and common arithmetic components (adder, subtractor, multiplier, comparator...).

Mark the name of every signal and indicate their width clearly.

Preferably write your answers in numerical order (1a, 1b, ... 5).

Please answer in Finnish if possible, eli vastaa suomeksi jos vain osaat.

1.   Answer and explain (6p)

   a)   Delta delay (2p)

   b)   Difference between terms `package` and `entity` in VHDL-language (2p)

   c)   What is the difference in using *generic* values or *constant* values? (2p)

2.   Analyze the code in the following page. The clock period is 10 ns. (9p)

   a)   What are the types of the processes: sequential or combinatorial? (1p)

   b)   Check and fix the sensitivity lists of the processes (1p)

   c)   What errors or suspicious structures there are still left in the code after task b? (3p)

   d)   Fill in the timing diagram below directly according the code, i.e., without correcting any errors. Present the timing as simulator interprets it. (4p)
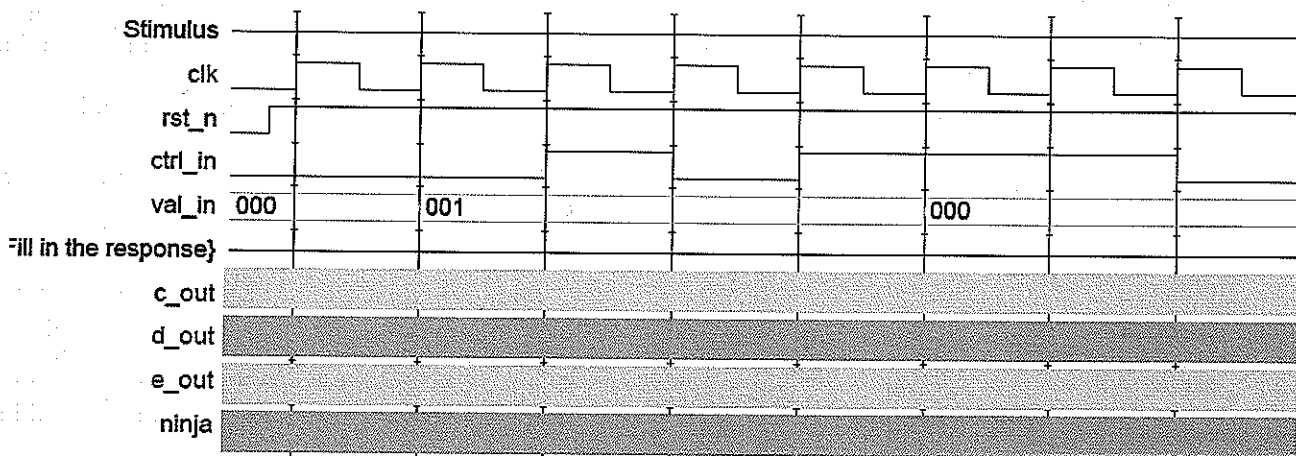
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```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity tentti is
  generic (
    data_width_g : integer := 3);
  port (
    clk     : in  std_logic;
    rst_n   : in  std_logic;
    ctrl_in : in  std_logic;
    val_in  : in  std_logic_vector (data_width_g-1 downto 0);
    c_out   : out std_logic;
    d_out   : out std_logic_vector (data_width_g-1 downto 0);
    e_out   : out std_logic_vector (data_width_g-1 downto 0)
    );
end tentti;

architecture gatelevel of tentti is

  signal ninja : unsigned ( data_width_g-1 downto 0);


begin

  tenho: process (ctrl_in, ninja, val_in)
  begin
    if ctrl_in = '1' then
     e_out <= not val_in after 4 ns;
    else
     e_out <= val_in after 4 ns;
    end if;
  end process tenho;

  sauren : process (clk, rst_n, ninja)
    variable tmp_v : unsigned (3-1 downto 0);
  begin
    if rst_n = '0' then
      ninja <= (others => '0');

    elsif clk'event and clk = '1' then
      tmp_v := ninja+1;
      d_out <= std_logic_vector(tmp_v);
      ninja <= ninja +2;

    end if;
  end process sauren;

  process (ninja)
  begin
    if to_integer (ninja) = 6 then
     c_out <= '1';
    else
     c_out <= '0';
    end if;
  end process;

  --c_out <= '0';

end gatelevel;
```

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3.   Analyze the VHDL code on the previous page. Show the resulting logic diagram after RTL syntehsis. Use dashed line to show separate synthesized logic of each process. Show every port, signal and variable. Don't make too small or ugly diagram, but clear and elegant. (6p)

4.   Reuse (5p)
    a)   List three basic forms of IP blocks in which they can be provided to integrator. Describe also their largest differences. (2p)
    b)   What is the type of block foo in Figure t4? (1p)
    c)   What are the benefits of reusing? (2p)

5.   Figure t5 shows an example SoC-chip. What things are important to describe about the block interface to the instruction manual of IP-block foo? (4p)
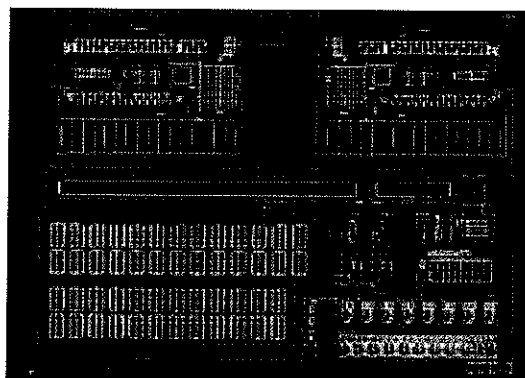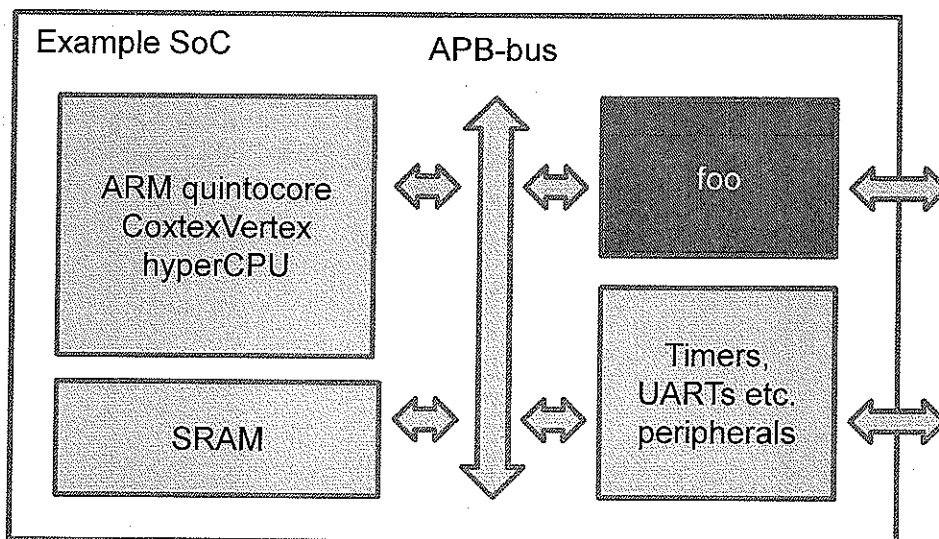

Figure t4. IP-block foo.

Figure t5. SoC. Concentrate on block foo.