

Name: _____

Student no. _____

Final Exam: Answer every question

2nd Midterm Exam: Answer only questions 3-5

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Students can use **any calculator** or dictionary.Moreover, each student can have 1 A4 sheet of **own notes**. There are no restrictions about their style and they are not collected.

Students can do anything they wish with the exam paper.

In addition to text, use figures, tables, equations, and examples in your answers.

In logic diagrams, you can use basic gates (AND, OR...), flip-flops, multiplexers, and common arithmetic components (adder, subtractor, multiplier, comparator...).

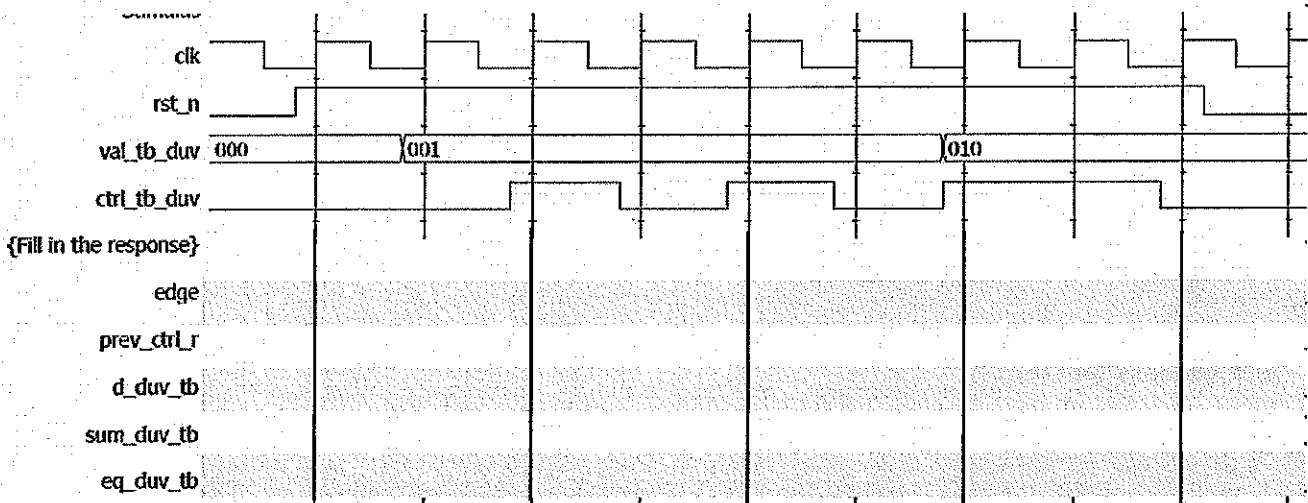
Mark the name of every signal and indicate their width clearly.

Preferably write your answers in numerical order (1a, 1b, ... 5).

Please answer in Finnish if possible, eli vastaa suomeksi jos vain osaat.

1. Answer and explain (6p)
 - a) Terms: signal's event and delta delay (2p)
 - b) What is the difference between VHDL structures package and entity? (2p)
 - c) What is so called *magic number*?

2. Analyze the code in the following page. The clock period is 10 ns. (7p)
 - a) What errors or suspicious structures there are in the code? (4p)
 - b) Fill in the timing diagram below directly according the code, i.e., without correcting any errors. Present the timing as simulator interprets it. (5p)



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```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use std.textio.all;
```

```
entity tentti_k14 is
```

```
  generic (
    data_width_g : integer := 8);
  port (
    clk           : in  std_logic;
    rst_n         : in  std_logic;
    ctrl_in       : in  std_logic;
    val_in        : in  std_logic_vector (data_width_g-1 downto 0);
    sum_out       : out std_logic_vector (data_width_g-1 downto 0);
    d_out         : out std_logic;
    eq_out        : out std_logic
  );
```

```
end tentti_k14;
```

```
architecture gatelevel of tentti_k14 is
```

```
  signal prev_ctrl_r : std_logic := '0'; -- delay reg
  signal edge        : std_logic;      -- detect falling edge
  signal sum_r       : integer;        -- accumulate
```

```
begin
```

```
  mike : process (clk, rst_n)
    variable sum : integer;
```

```
  begin
```

```
    if rst_n = '0' then
      sum_r <= 0;
      d_out <= '0';
```

```
    elsif clk'event and clk = '1' then
      d_out <= '0';
      prev_ctrl_r <= ctrl_in;
      d_out <= prev_ctrl_r;
```

```
    if edge = '1' then
      sum_r <= to_integer(unsigned (val_in)) + sum_r;
    end if;
```

```
  end if;
```

```
end process mike;
```

```
sum_out <= std_logic_vector (to_unsigned (sum_r, data_width_g));
```

```
patton : process (val_in, ctrl_in, prev_ctrl_r, rst_n)
begin
```

```
  if (prev_ctrl_r = '0' and ctrl_in='1') then edge <= '1';
  else edge <= '0';
  end if;
```

```
  if std_logic_vector (to_unsigned (sum_r, data_width_g)) = val_in then
    eq_out <= '1';
  else
    eq_out <= '0';
  end if;
```

```
end process patton;
```

```
end gatelevel;
```

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3. Analyze the VHDL code on the previous page. Show the resulting logic diagram after RTL synthesis. Use dashed line to show separate synthesized logic of each process. Show every port, signal and variable. Don't make too small or ugly diagram, but clear and elegant. (6p)
4. Reuse (4p)
 - a) List three basic forms of IP blocks in which they can be provided to integrator. Describe also their largest differences. (2p)
 - b) What is the type of block foo in Figure t4? (1p)
 - c) What are the benefits of reusing? (1p)

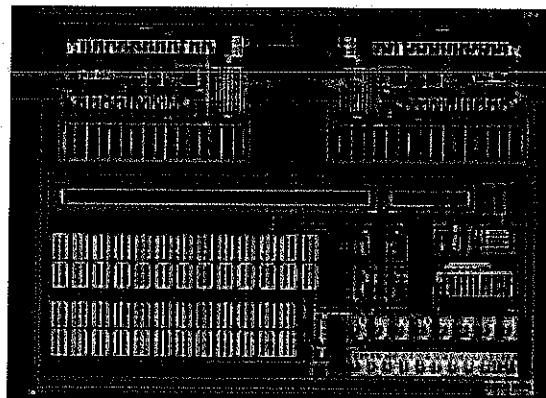


Figure t4. IP-block *foo*.

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5. Analyze the test circuit below (5p)
- How the metastability is detected in basic RTL-simulation? (2p)
 - How the test circuit works? (Hint: in addition to text, draw a small timing diagram where something interesting happens) (3p)

Figure 4. Test Circuit Structure for Metastability Characterization

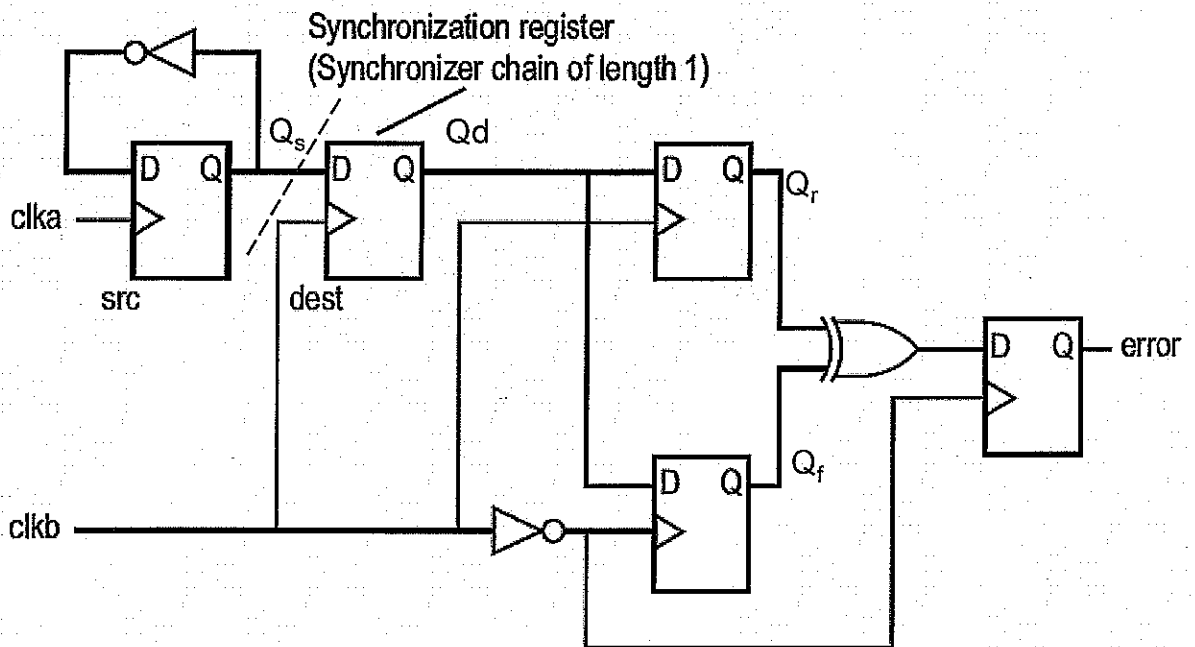


Figure t5. Test Circuit