TIE-50206 Logic Synthesis, Final Exam / Midterm Exam 2
Thu 1.3.2018 Page 1/3

Name: ______________________________

Student no. ______________________________

Final Exam: Answer every question

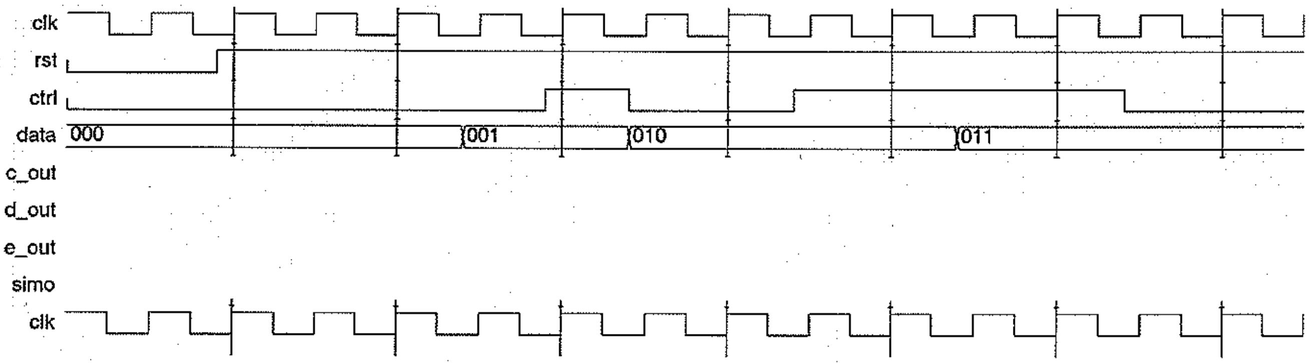
2nd Midterm Exam: Answer only questions 3-5

Made by: Arto Perttula
Students can use **any calculator** or dictionary.
Moreover, each student can have 1 A4 sheet of **own notes**. There are no restrictions about their style and they are not collected.
Students can do anything they wish with the exam paper.

In addition to text, use figures, tables, equations, and examples in your answers.
In logic diagrams, you can use basic gates (AND, OR...), flip-flops, multiplexers, and common arithmetic components (adder, subtractor, multiplier, comparator...).
Mark the name of every signal and indicate their width clearly.
Preferably write your answers in numerical order (1a, 1b, ... 5).
Please answer in Finnish if possible, eli vastaa suomeksi jos vain osaat!

1. Answer and explain (6p)
   a) Delta delay (2p)
   b) Difference between terms `package` and `entity` in VHDL-language (2p)
   c) What is the difference in using *generic* values or *constant* values? (2p)

2. Analyze the code in the following page. The clock period is 10 ns. (9p)
   a) What are the types of the processes: sequential or combinatorial? (1p)
   b) Check and fix the sensitivity lists of the processes (1p)
   c) What errors or suspicious structures there are still left in the code after task b? (3p)
   d) Fill in the timing diagram below directly according the code, i.e., without correcting any errors. Present the timing as simulator interprets it. (4p)



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```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity tentti is
  generic (
    data_width_g :     integer := 3);
  port (
    clk          : in  std_logic;
    rst          : in  std_logic;
    ctrl         : in  std_logic;
    data         : in  std_logic_vector (data_width_g-1 downto 0);
    c_out        : out std_logic;
    d_out        : out std_logic_vector (data_width_g-1 downto 0);
    e_out        : out std_logic_vector (data_width_g-1 downto 0)
    );
end tentti;


architecture structural of tentti is

  signal simo : std_logic_vector ( data_width_g-1 downto 0);


begin

  d_out <= simo after 2 ns;

  spede: process (data)
  begin
    if ctrl = '1' then
      c_out <= data (1) or data (0);
    else
      c_out <= data (1) and data (0);
    end if;
  end process spede;

  vesku : process (clk, rst, data)
  begin
    if rst = '0' then
      simo <= "000";

    elsif clk'event and clk = '1' then

      if ctrl = '1' then
        simo <= data;
      else
        simo <= "ZZZ";
      end if;
    end if;
  end process vesku;

  ronnie_r: process (clk, rst)
    variable tmp_v : std_logic_vector ( data_width_g-1 downto 0);
  begin  -- process ronnie_r
    if rst = '0' then

    elsif clk'event and clk = '1' then
      tmp_v := simo;
      e_out <= tmp_v;
    end if;
  end process ronnie_r;

end structural;
```

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3. Analyze the VHDL code on the previous page. Show the resulting logic diagram after RTL syntehsis.Use dashed line to show separate synthesized logic of each process. Show every port, signal and variable. Don't make too small or ugly diagram, but clear and elegant. (6p)

4. Reuse (5p)

   a) List three basic forms of IP blocks in which they can be provided to integrator. Describe also their largest differences. (2p)

   b) What is the type of block *foo* in Figure t4? (1p)

   c) What are the benefits of reusing? (2p)

5. Analyze the circuit below in Figure t5 (4p)

   a) Which signals have to be synchonized? Or is it necessary to synchronize any of them? (2p)

   b) Is there enough signals for proper working? (2p)

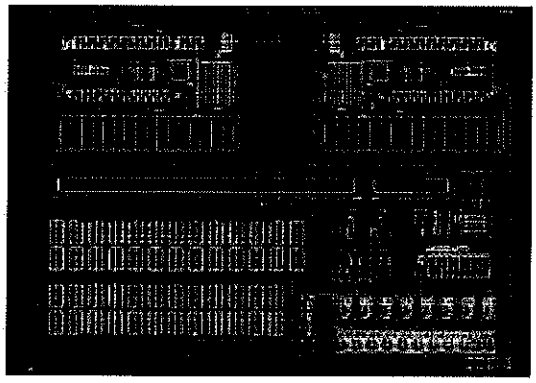

Figure t4. IP-block *foo*

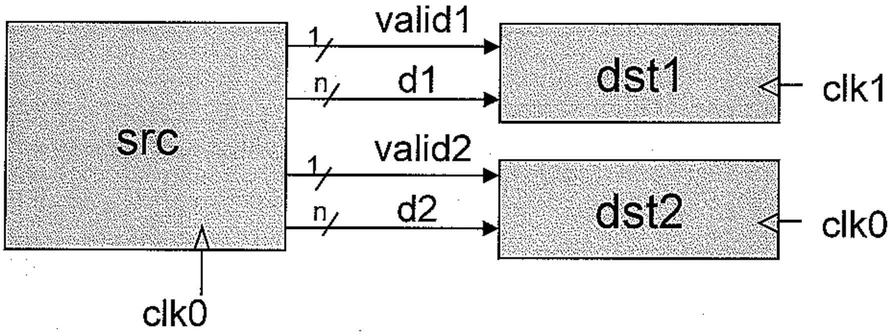

Figure t5. Synchronization between clock domains